INSTRUCTION MANUAL

CAPACITANCE LOSS METER

TYPE CLM 1

Contents:
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1. Introduction

The CLM 1 is a four-terminal loss factor meter measuring tanδ directly in % at a measuring frequency of 100 kHz.

The four-terminal arrangement eliminates measuring errors due to varying contact resistance in a test jig or an automatic sorting machine and makes it possible to measure tanδ with an accuracy of 10^{-4}.
100 kHz has been chosen as test frequency in order to perform accurate measurements of small variations of series resistance originating from differences in contact resistance between leads and foil. Losses due to contact resistance become more significant at 100 kHz and can be measured with higher accuracy than with the standard test frequency of 1 kHz.

The instrument is supplied in a cabinet with a width 2/3 of a 19 inch standard cabinet (a full 19 inch cabinet is optionally available) with a four-terminal test jig and a measuring cable from main frame to jig or test station fitted with BNC connectors.
The cable length is 1 meter allowing the CLM 1 to be connected to a sorting machine or to capacitors placed in a test chamber. Readout is provided on a panel meter and two analog outputs are available.

The instrument is supplied with a built-in analog limit comparator with a digital knob on the front panel for setting maximum tanδ. Green and red LEDs on the front panel indicate the ACCEPT/REJECT condition and a switch output is available.

Specifications

Measuring Frequency:	100 kHz ±0.1%
Capacitance Range:	100 pF - 25 µF in four ranges 100 pF - 1 nF, 1 nF - 30 nF, 30 nF - 1 µF and 1 µF - 25 µF.
Tanδ Accuracy:	100 pF - 30 nF: 1×10^{-4} 30 nF - 1 µF: 3×10^{-4} 1 µF - 25 µF: ~~5~~ $\times 10^{-4} + C(\mu F) \times 10^{-4}$

Meter Display:	Four ranges: 0.3, 1, 3 and 10% tanδ full scale.
Meter Display Accuracy:	±2% reading ±1% of full scale.
Measuring Voltage:	Max. 1 V rms.
Settling Time:	Max. 50 milliseconds.
Analog Outputs:	+10 V for full scale meter deflection, -1 V/% absolute tanδ. (Min. 2 kΩ external load).
Terminals:	Four-terminal connection with guard voltage on the shields of terminal 3 and 4.
Test Jig:	Detector and generator terminal are 4 mm jacks with 19 mm spacing to enable the use of standard component fixtures.
Limit Output:	Open collector (standard) rating 35 V/0.5 A max. 3 watt. Cam relay (optional) with double shift-over contact rated 220 V/5 A max. 500 VA.
Power:	100 - 130 V and 200 - 260 V AC 50 - 60 Hz, consumption 10 VA.
Total Net Weight:	5.1 kilos.
Dimensions:	Height 147 mm, width 325 mm, depth 356 mm. 19 inch cabinet for rack mounting optional.
Accessories supplied:	One pair of fixtures for axial-lead components. One fixture for radial-lead components. One power lead.

2. Operating Instructions

2.1. Setting Up

Check that the mains voltage selector is set to the actual supply voltage. The selector switch is located on the rear panel. Changing of the setting: Pull the knob, turn to the correct position and push back. Check that a 0.5 A slow-blow fuse is fitted.

Connect the test jig or test station to the main frame with the measuring cable according to the number indications. Note that two sets of Generator/ Reference terminals are provided on the test jig to enable measurements on capacitors of different lengths.
If a test station is used, please remember that the shields on terminal 3 and 4 are guarded and that the shield on terminal 1 must not be connected to earth on the test station. The shield on terminal 2 may be used as a ground connection from the main frame to test station.

As a four-terminal arrangement is used, the terminal 1 and 2 and the terminal 3 and 4 respectively must be interconnected before any checks or measurements are possible. When using the test jig and the test fixtures supplied by Danbridge, the terminals are automatically interconnected.

2.2. Initial Calibration

Set the Controls as follows:

Range Switch:	1 nF - 30 nF
Meter Switch:	0.3% f.s.

Switch on the equipment and allow at least half an hour's stabilisation before calibration.
Push the right push-button "ADJ. 0.2%" and adjust the corresponding potentiometer with a small screw-driver to 0.2% reading on the meter.
Push the left push-button "ADJ. 0.2%" and adjust the corresponding potentiometer to 0.2% reading on the meter.

When changing from the supplied test jig to a test station e.g. on a sorting machine it may be necessary to readjust the main frame (connected to the test station) as described in the 'Maintenance Instructions' Section 4.2.

2.3. Measurements

Place the capacitor in the measuring jig. Set the range switch to the appropriate capacitance range and switch the meter switch to maximum reading within scale.

2.3.1. Measurement Errors

When other test jigs than those supplied are connected to the terminals of the measuring cable, please keep in mind that the lead length between the terminals and the contacts should be as short as possible, and that additional ground capacitance should be avoided. These capacitances cause a measuring error, especially any capacitance to terminal 3 and 4. The error is largest on the 100 pF - 1 nF range, e.g. with a 100 pF in the test jig, 18 pF between terminal 4 and ground gives about 0.025% low tanδ reading.

If the test jigs used do not provide any connection between terminals 3 and 4 with no measuring capacitor in circuit some drift may appear on the lowest ranges if the contacts are left open for more than a few seconds.
To eliminate this drift a resistor of about 100 Ohms may be connected between the terminals 3 and 4, as close as possible to the actual terminals.

2.3.2. Analog Output

Two analog outputs are available at the rear output connector. One giving +10 V for full scale meter deflection. This may be employed, e.g. for driving a remote meter or an external limit selector when high output at small values of tanδ is required. The second output is directly proportional to tanδ giving -1 V for tanδ equal to 1% and may be employed to drive an external limit selector.

3. Circuit Description

Diagrams 1 & 2

The Generator supplies the measuring voltage 1 V rms. across the capacitor with unknown loss factor C_x in series with a standard resistor R_n. The voltages across C_x and R_n, the amplitude of which are a function of the capacitance of C_x, are fed into two phase-lock loop circuits PLL2 and PLL1 respectively.

The PLL circuits transform the sinusoidal signals into squarewaves with constant amplitude in precise phase-quadrature to the incoming signals. The squarewaves are fed into the Main Detector whose output is proportional to the phase difference between the squarewaves -90^{o}, i.e. proportional to $\tan\delta$.

The Main Detector output supplies -1 volt per % absolute $\tan\delta$ for the Limit Comparator and the Meter Amplifier.

3.1. Details of Circuit

3.1.1. The Measuring Circuit

Diagrams 3 & 4

The measuring voltage across C_x in series with R_n is supplied from the Generator via transformer L 401. The junction between C_x and R_n is connected to the inverting input of an operational amplifier CA 3030A, IC 403. The output of IC 403 is connected to the centre tap of the secondary of L 401. This makes the input a virtual earth at zero potential which minimizes errors due to stray capacitance and cable capacitance from terminal 1 and 2 to ground.
A current, taken from the output of IC 403 set by RV 403 and fed via R 411 into the inverting input of IC 403, compensates capacitive currents from terminal 4 to ground in order to eliminate errors at low value capacitor measurement.

In order to perform a true four-terminal measurement, the residual voltage at terminal 4 is fed to PLL 2 via the voltage follower LM 310, IC 401. A guard voltage taken from the low impedance output of IC 401 is supplied via R 401 to the shield of the coax-cable to terminal 4, thus reducing the cable capacitance to ground.

In order to avoid errors at high value capacitor measurements due to cable inductance, the voltage at D is fed into PLL 2 via the voltage follower LM 310, IC 402. A guard voltage taken from the output is supplied via R 402 to the shield of the coax-cable from D to terminal 3 reducing the cable capacitance to ground.

The standard resistors are mounted on a separate PC board on the Capacitance Range Switch. R_{N2}, R_{N3} and R_{N4} are separately shunted by an R-C network, compensating phase errors in the individual capacitance ranges due to shunt capacitances across the standard resistors.

It has been necessary to choose a value of R_{N1} lower than the optimum to ensure stability of the Measuring Circuit. This causes the voltage across R_{N1} for C_x < 400 pF to be too low to ensure the prescribed phase stability of PLL1.
To overcome this problem the voltage across R_{N1} is amplified by the operational amplifier CA 3030A, IC 404 before it is fed to PLL1, when the Range Switch is in position 100 pF - 1 nF.

The Measuring Circuit has two built-in loss factor standards for adjustments. They are switched in between D and B with the adjust switches on the front panel, i.e. they are placed across the Detector and Generator Terminals of the test jig.

Each loss factor standard consists of one or more very low loss capacitors shunted by a resistor network adjusted to give a tanδ reading of 0.2% on the meter with the Range Switch in position 1 nF - 30 nF.

3.1.2. The PLL Circuit

Diagrams 5 & 6

The phase-lock loops PLL1 and PLL2 convert the sinusoidal voltages across R_N and C_x to squarewaves with 50% duty cycle, very small rise and fall times, constant amplitude and almost exactly in phasequadrature with the sinusoidal input signals.

PLL1 and PLL2 consist of a phase detector, a level shifter, a voltage-controlled oscillator and a flip-flop. As they are identical, only one, the PLL2 will be described in detail.

The phase detector is designed with the monolithic balanced modulator/detector MC 1596, IC 201.
To bias it and enhance its performance the following circuits are added. A 12.1 kΩ resistor R 215 to pin 5 sets the D.C. currents in the two branches to approx. 1.2 mA. The lower differential inputs - the signal port - are biased with two resistor networks, one of them variable to balance the D.C. currents through the transistors.
The 3.16 kΩ resistor R 213 between pin 2 and 3 (i.e. the emitters of the input transistors) sets the transadmittance of the signal stage.
The switching inputs are supplied with the squarewave outputs of the flip-flop IC 204.
The outputs (the crosscoupled collectors of the switching transistors) are current-feeding an operational amplifier IC 202, which adds gain and shifts the voltage level to an appropriate level for the control input of the voltage controlled oscillator (VCO).

The collector resistors R 214 and R 218 are matched to within 0.1% and to within 5 ppm in temperature coefficient in order to reduce offset and temperature drift at the inputs of the amplifier. A balancing network is further applied to the collectors - R 216, R 217 and RV 202 - to increase common mode rejection. The potentiometer is set to keep the output of IC 203 constant when varying the current into pin 5 of IC 201 and thereby the D.C. currents through the device.
The 2.2 µF capacitors, C 210 and C 311, decouple the A.C. components of the collector currents.

The levelshifter employs an integrated operational amplifier LM 725C, IC 202, because of its very low input offset voltage drift and input offset current, its high open loop gain and common mode rejection, and low input noise.
The amplifier is provided with an external offset null network by means of which it is possible to

minimize the offset voltage drift. The R-C network in the feedback - and the similar one connected to the non-inverting input - sets the first pole and zero in the PLL loop, and sets the gain of the amplifier to approx. 1 V/µA.
The front-panel potentiometer RV 203 sets the voltage level at the output of the amplifier and hence the free-running frequency of the VCO, thus making it possible to adjust the phase error of the loop.

The output of the amplifier is fed to the control input of the VCO via R 229 and R 230 shunted by C 220. The junction point between R 229 and R 230 is clamped to the 5 V supply voltage with the diodes D 201 and D 202. This limits the D.C.-control voltage to the VCO and ensures that the PLL is unable to lock on harmonics of the input frequency.

The VCO is a monolithic voltage-controlled oscillator XR 2207CP, IC 203 with excellent frequency stability. The free-running frequency is set by the polystyrene capacitor C 223 and the control voltage at pin 6 - the control input - to approx. 200 kHz.
The voltage to frequency conversion gain K_O is controlled by C 223 and R 229 + R 230.
The squarewave output of IC 203 is fed to the clock input of the toggling flip-flop IC 204, which divides the VCO frequency by 2. The Q and $\overline{Q}$ outputs of the flip-flop are fed back to the switching input of IC 201 through C 202 and C 201 thus closing the loop.

The flip-flop IC 204 is a schottky-clamped dual J-K flip-flop SN 74S113N. By setting the J, K, and preset inputs "high", the device forms a frequency divider. The squarewave outputs Q and $\overline{Q}$ have exact 50% duty cycle and very small rise- and falltimes, which is necessary in order to minimize the effects of offset voltages on the switching inputs of - and the current imbalance in - the detectors.

3.1.3. The Main Detector

Diagram 7

The Main Detector consists of a phase detector and a level shifter. The phase detector is identical with the phase detectors in the PLL circuits described above, except for the gain setting resistor R 313 between pin 2 and 3.
The level shifter is designed with the operational amplifier LM 301A, IC302. The R-C networks C 316 - R 326 and C 313 - R 325 set the gain of the level shifter and supply the output with the necessary noise suppression.
In addition they set the dominant pole of the total system, i.e. control the settling time.

RV 303 corrects the operational amplifier offset and hence the offset of the Main Detector.

3.1.4. The Meter Amplifier

Diagram 8

The output of the Main Detector is applied to the Meter Switch, the four resistors of which control the gain of the operational amplifier LM 301A, IC 501.
The output of IC 501 is fed to the tanδ Meter via RV 502 shunted by R 511 and R 512.
RV 502 sets the correct meter deflection - full scale for 10 V at pin 6 of IC 501 - and D 501 connected between pin 6 and ground protects the meter against negative voltage excursions.

3.1.5. The Generator

Diagram 9

The Generator consists of an oscillator and an output amplifier. It supplies the Measuring Circuit with a 100 kHz 1 V rms sinewave via transformer L 401.
This sinewave must be very pure in order to avoid measuring errors due to odd harmonics. To achieve this a high-Q tuned circuit (Q about 300) is employed in the oscillator. This also ensures a good frequency stability determined mainly by the components of the tuned circuit.

The oscillator is designed with a tuned circuit and the transistor array CA 3054, IC 701 consisting of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate.
Only one of the amplifiers is used in a cascode configuration with positive feed-back. Q_2, one of the two common-base stages (formed by the differential pair Q_1 and Q_2) is used as a gain control.
The collector of Q_1 feeds the tuned circuit - L 701 and C 708 - via a link (winding ratio 10:106) and another link (1 winding) delivers the positive feed-back signal to the base of Q_3.

The voltage of the tuned circuit is applied to the non-iverting input of operational amplifier LM 318, IC 702 which together with a push-pull stage constitutes the output amplifier. The output of IC 702 is supplied to the amplitude detector D 701, R 701 and C 701. The detector output is fed via RV 701 to the base of the gain control transistor Q_2. RV 701 sets the amplitude of the Generator output signal.
IC 702 feeds the push-pull stage formed by Q 702 and Q 703 and biased by Q 701. The push-pull output voltage is fed back to the inverting input of IC 702 via the resistive divider R 707 and R 706 in order to minimize the total harmonic distortion of the output amplifier.

The output amplifier is able to deliver 1 V rms/500 mA via the transformer L 401 (see diagram 3) to the Measuring Circuit.

3.1.6. The Limit Comparator

Diagram 10

A voltage proportional to tanδ supplied from the Main Detector is fed into the non-inverting input of operational amplifier LM 301A, IC 601. IC 601 is connected as a voltage comparator. A small amount of hysteresis (approx. 7 mV tanδ equal to 0.007%) is provided by positive feed-back from the output via R 605 to the non-inverting input. R 601 in series with the front-panel mounted 10 turn potentiometer RV 601 connected between -15 V and ground form a

voltage divider. The voltage level at the arm of RV 601 is fed via R 604 to the inverting input of IC 601 as a reference voltage. The digital knob mounted on RV 601 sets the maximum value of tanδ.

The output of IC 601 feeds the base of the LED-driver transistor Q 601 and the output darlington transistor Q 602. The collector of R 602 is connected to pin 5 at the rear panel socket.
When the Main Detector output is more positive than the reference voltage, i.e. when tanδ is lower than the preset value, the output of IC 601 goes "high" and the collectors of Q 601 and Q 602 go "low" turning on the green LED 601 mounted on the front panel. The voltage level at the junction point K between R 608 and LED 601, which feeds the base of LED-driver Q 603 via R 609 goes "low" cutting R 603 off.

When the Main Detector output is more negative than the reference voltage, i.e. when tanδ is higher than the preset value, the output of IC 601 goes "low" and the collectors of Q 601 and Q 602 go "high". Q 603 saturates and the red front-panel mounted LED 602 switches on.

A cam relay with double shift-over contacts (rated 220 V/5 A max. 500 VA) is optionally available. The CLM 1 is prewired for the cam relay (Siemens V23154 D0717-F104) and the relay socket is mounted as standard.

N.B.: When the cam relay is mounted, loads connected between the open collector output at pin 5 and supply voltages lower than +15 V may cause malfunction of the relay.

3.1.7. The Power Supply

Diagram 11

The regulators for the power supply voltages (±15 V and +5 V) are placed on two PC boards mounted on the rear panel together with the power transformer, the line voltage selector, the fuse, and the line voltage input socket.

The ±15 V supply is designed with an integrated dual-voltage regulator driving the two power transistors MJE 3055 and MJE 2955, which use the rear panel as heatsink. Two potentiometers control the output voltage values and balance respectively.

The +5 V supply is independent of the ±15 V supply and designed with the integrated regulator LM 723 driving the MJE 2955 output transistor. A potentiometer for precise output voltage setting is provided.

4. Maintenance Instructions

The adjustments by the two front-panel controls - as described in the Operation Instructions - should suffice for a trouble-free long term use. If a test station or test jig with longer leads than those supplied with the test jig is used, or if a degrading of the measuring accuracy appears, which cannot be countered by the front-panel adjustments, a realignment of the factory-set potentiometers inside the apparatus may be necessary as described in section 4.2.
In case of repair, a realignment of the individual circuits may be necessary as described in section 4.1., followed by a realignment of the whole system as described in section 4.2.

The user is warned:

Follow the instruction manual carefully and do not replace the matched resistors (R 114, R 118 and R 214, R218) or the balanced modulators MC1596 (IC 101 and IC 201) in the PLL circuits by others than the appropriate spare parts delivered by Danbridge.

If an adjustment is made it is necessary to use a digital voltmeter (DVM), an amplifying AC-voltmeter (AVM), a frequency counter, an oscilloscope with a high impedance probe, and four capacitors with known very small loss factors at 100 kHz ($\tan\delta < 0.1\%$) and values of 100 pF, 1 nF, 5.6 nF and 30 nF.

In order to obtain easy access to the PC boards loosen the four screws in each corner of the front panel and pull the main frame out from the cabinet.

4.1. Alignment of Individual Circuits

4.1.1. Supply Voltage Adjustment

The ±15 V supply on PC board 89207, mounted on the rear panel, is adjustable with two single-turn potentiometers. The right-hand potentiometer (seen from the

upper side) sets the positive voltage, and the left-hand potentiometer sets the balance. The +15 V and the -15 V should not deviate more than a few millivolts from the nominal values.

The +5 V supply on PC board 89216 A, mounted on the rear panel, is set to +5.10 volt by the 1 kΩ single-turn potentiometer in order to supply the correct clamp-voltage to the PLL circuits.

4.1.2. Adjustment of the PLL Circuits

As PLL 1 and PLL 2 are identical, only the adjustment of PLL 2 will be described.

If the measuring cable and the test jig with its test fixtures are disconnected, then connect on the main frame terminal 1 to terminal 2 and terminal 3 to terminal 4 with coax-cables.

Remove IC 701 from the Generator to secure that no signal is applied to the signal port of the phase detector IC 201.
Remove the filter capacitor C 211 from IC 201 pin 9, and short the switching output of IC 201 (pin 6 to pin 9).
Measure V_{io}, the voltage difference between IC 202 pin 6 and the arm of RV 203 (the junction point between R 224 and C 212), with the DVM and adjust RV 204 to Zero V_{io} reading.
Remove the short from the switching output and connect a counter (or oscilloscope) to IC 204 pin 1.
Adjust the left "ADJ. 0.2%" potentiometer on the front panel to 200 kHz counter reading (within ±2%).

Connect the oscilloscope to IC 201 pin 9 and observe the squarewave feedthrough. Adjust RV 201 to minimum feedthrough.
Reinsert the filter capacitor C 211.

The balancing network applied to the switching output of IC 201 (R 216, R 217 and RV 202) must be adjusted to keep the output constant when the current into pin 5 is varied and thereby the DC current through the device. This is carried out as follows:
Connect the DVM to the output of IC 202 (pin 6).

Observe the DVM reading. Shunt R 215 with a 100 kΩ resistor and observe the DVM reading. Adjust RV 202 to the same reading with and without the 100 kΩ shunt.

4.1.3. Adjustment of the Main Detector

Insert IC 701 in the Generator and check the Generator frequency (100 kHz ±0.1%).
Remove IC 203 from PLL 2 and the filter capacitor C 312 from IC 301 pin 9.
Connect the oscilloscope to IC 301 pin 9 and observe the carrier feedthrough. Adjust RV 301 to carrier null.
Reinsert the filter capacitor C 312.

The adjustment of the balancing network applied to the switching output of IC 301 (R 316, R 317 and RV 302) is carried out by using the same procedure as in the PLL circuits (see above).

4.1.4. Adjustment of the Generator

Connect the counter to the Generator output (the junction point between R 712 and R 713). Adjust the frequency to 100.00 kHz with the inductance adjustor in the oscillator coil.
Connect the AVM to the Generator output and adjust the output amplitude to 7 V rms with the amplitude control potentiometer RV 701.

4.1.5. Adjustment of the Meter Amplifier and the Limit Comparator

Set the controls as follows:

Range Switch	1 nF - 30 nF
Meter Switch	1% fs.

Connect the DVM to the Main Detector output (the rear panel socket pin 3). Push one of the "ADJ. 0.2%" switches and observe the DVM reading.
Connect the DVM to the Meter Amplifier output (the rear panel socket pin 4). Push the switch again and adjust RV 501 until the DVM shows - 10x the previous DVM reading.

Switch the Meter Switch to 0.3% f.s. With the DVM connected to the rear panel socket pin 4, push one of the "ADJ. 0.2%" switches, set RV 303 (in the Main Detector) to 9.49 V DVM reading, and adjust RV 502 to 0.3% tanδ Meter reading.

4.2. Alignment of Measuring Circuit and the Complete System

Connect the test jig or test station to be used to the main frame via the Measuring Cable and set the controls as follows:

Range Switch:	1 nF - 30 nF
Meter Switch:	0.3% f.s.

a. Mount the 5.6 nF capacitor C_1 in the test jig. Offset the Main Detector output to 0.1% meter reading with the offset potentiometer RV 303 (in the Main Detector).

Mount the 1 nF capacitor C_2 in the test jig. Adjust the right "ADJ. 0.2%" potentiometer RV 103 on the front panel (with a screwdriver) until the correct loss factor difference appears on the meter when switching from C_1 to C_2.

Example: Let the loss factor of C_1 be 0.03% and the loss factor of C_2 be 0.01%. Then the correct adjustment of R 103 would cause a difference between the two meter readings of - 0.02%, when C_1 is replaced by C_2 in the test jig.

b. Mount C_1 in the test jig and reset RV 303 to 0.1% meter reading. Replace C_1 by the 30 nF capacitor C_3. Adjust the left "ADJ. 0.2%" potentiometer RV 203 until the correct loss factor difference appears on the meter when switching from C_1 to C_3.

Repeat point a. and b. until correct loss difference appears on the meter in both cases.

c. Switch the Range Switch to 100 pF - 1 nF.
Mount C_2 in the test jig and adjust RV 303 for 0.1% meter reading.
Replace C_2 by the 100 pF capacitor C_4. Adjust RV 403 until the correct loss difference appears on the meter when switching from C_2 to C_4.

If more than a very small adjustment ($2 - 3 \times 10^{-4}$) is necessary repeat a., b., and c.
Mount C_2 in the test jig and observe the meter reading. Switch the Range Switch to 1 nF - 30 nF. Adjust RV 801 (the left potentiometer on the standard resistor PC board) for identical meter readings.

Mount C_3 in the test jig and observe the meter reading. Switch the Range Switch to 30 nF - 1 µF. Adjust RV 802 (the second potentiometer from the left on the standard resistor PC board) for identical readings.

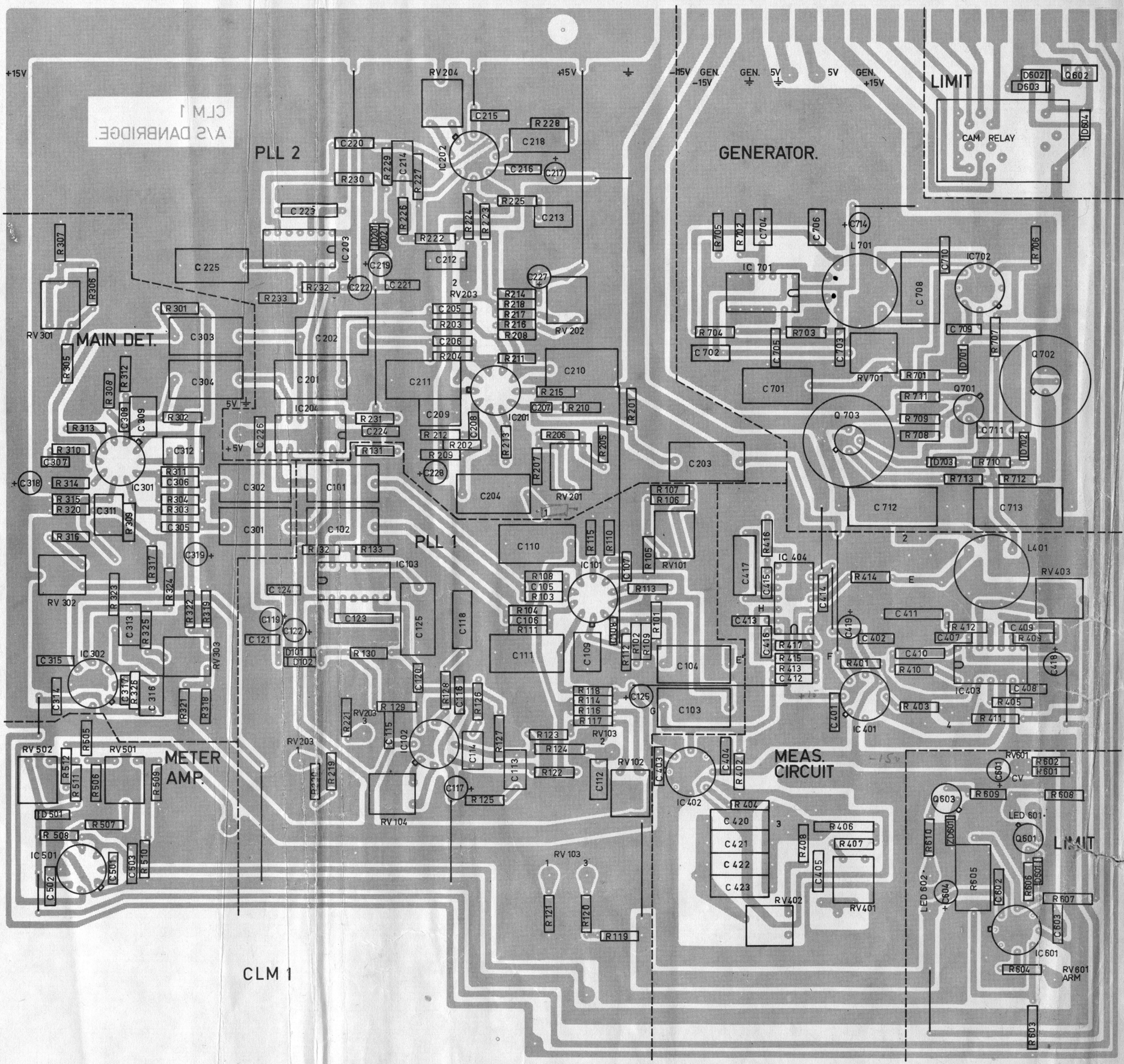
Mount a 1 µF capacitor (use a polycarbonate capacitor with a small loss factor for highest accuracy) in the test jig.
Switch the Meter Switch to the appropriate range and observe the meter reading. Switch the Range Switch to 1 µF - 25 µF.
Adjust RV 803 (the right-hand potentiometer on the standard resistor PC board) for identical readings.

Set the Range Switch in position 1 nF - 30 nF and the Meter Switch to position 0.3% f.s.
Mount C_1 in the test jig and adjust RV 303 (in the Main Detector) for the correct meter reading (the correct absolute value of tanδ).

Remove C_1 from the test jig and make sure that terminal 1 is shorted to terminal 2 and terminal 3 shorted to terminal 4 by the test fixtures.

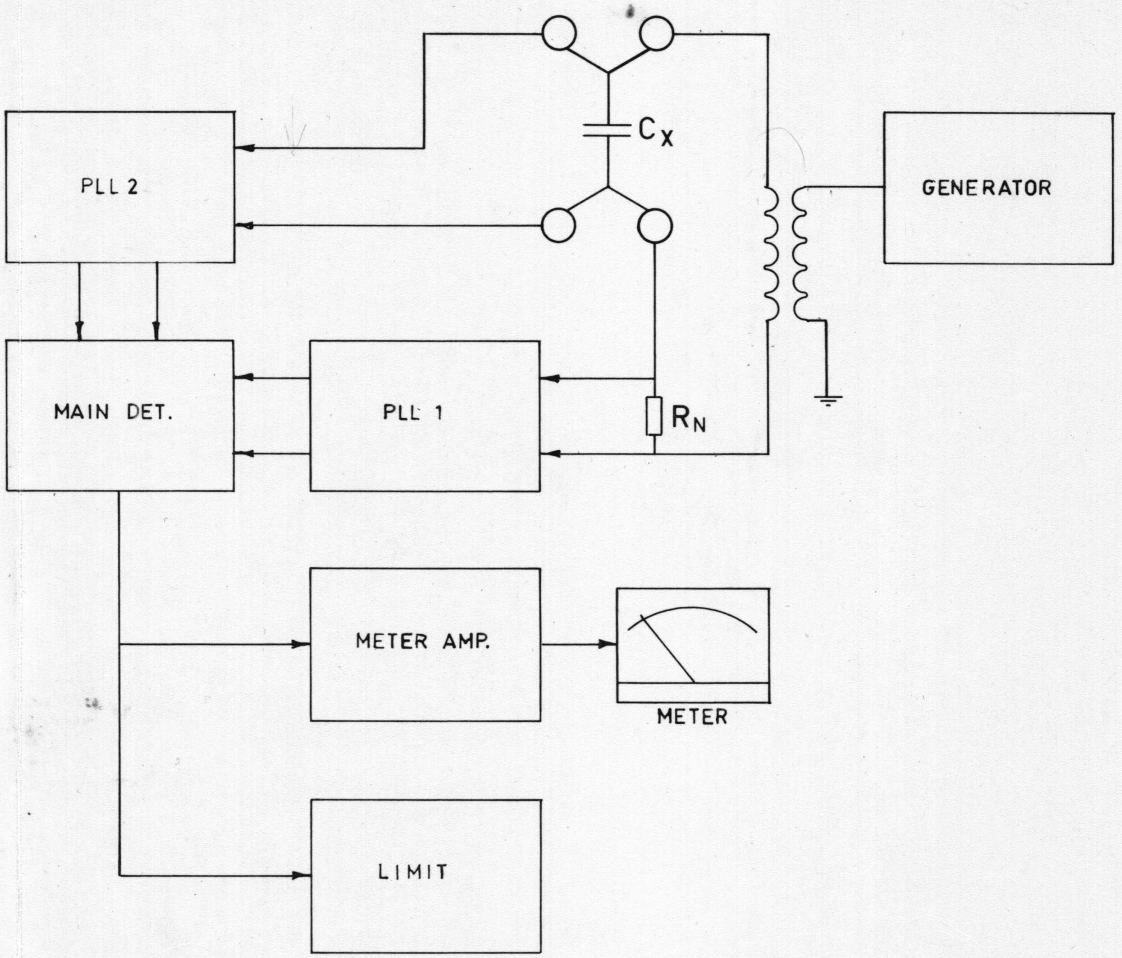
Push the right-hand "ADJ. 0.2%" pushbutton and adjust RV 401 (mounted on the main PC board) to 0.2% meter reading.

Push the left-hand "ADJ. 0.2% pushbutton and adjust RV 402 to 0.2% meter reading.

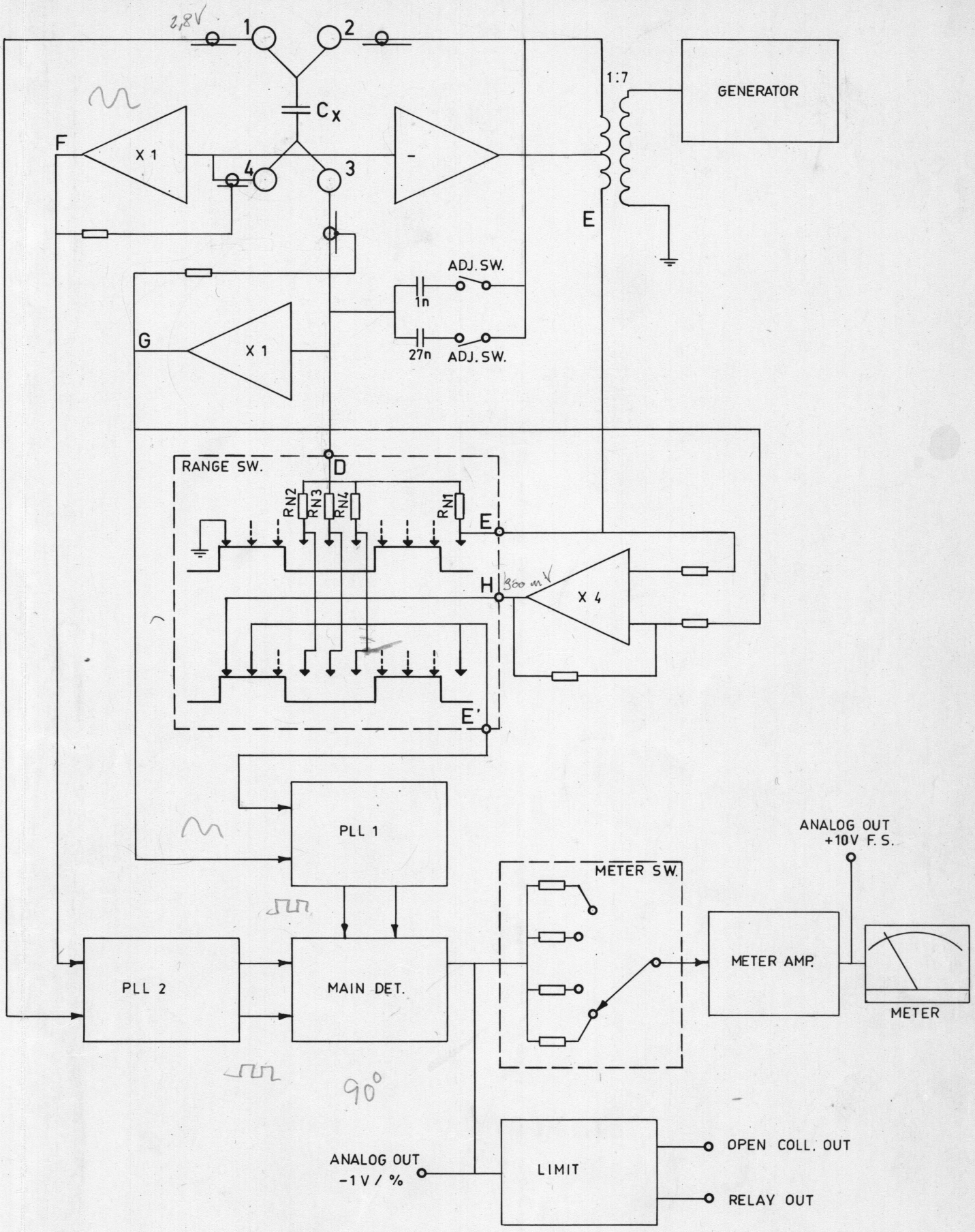


KOMPONENTPLAN. TEGN.: 130176 B.ras GODK.:

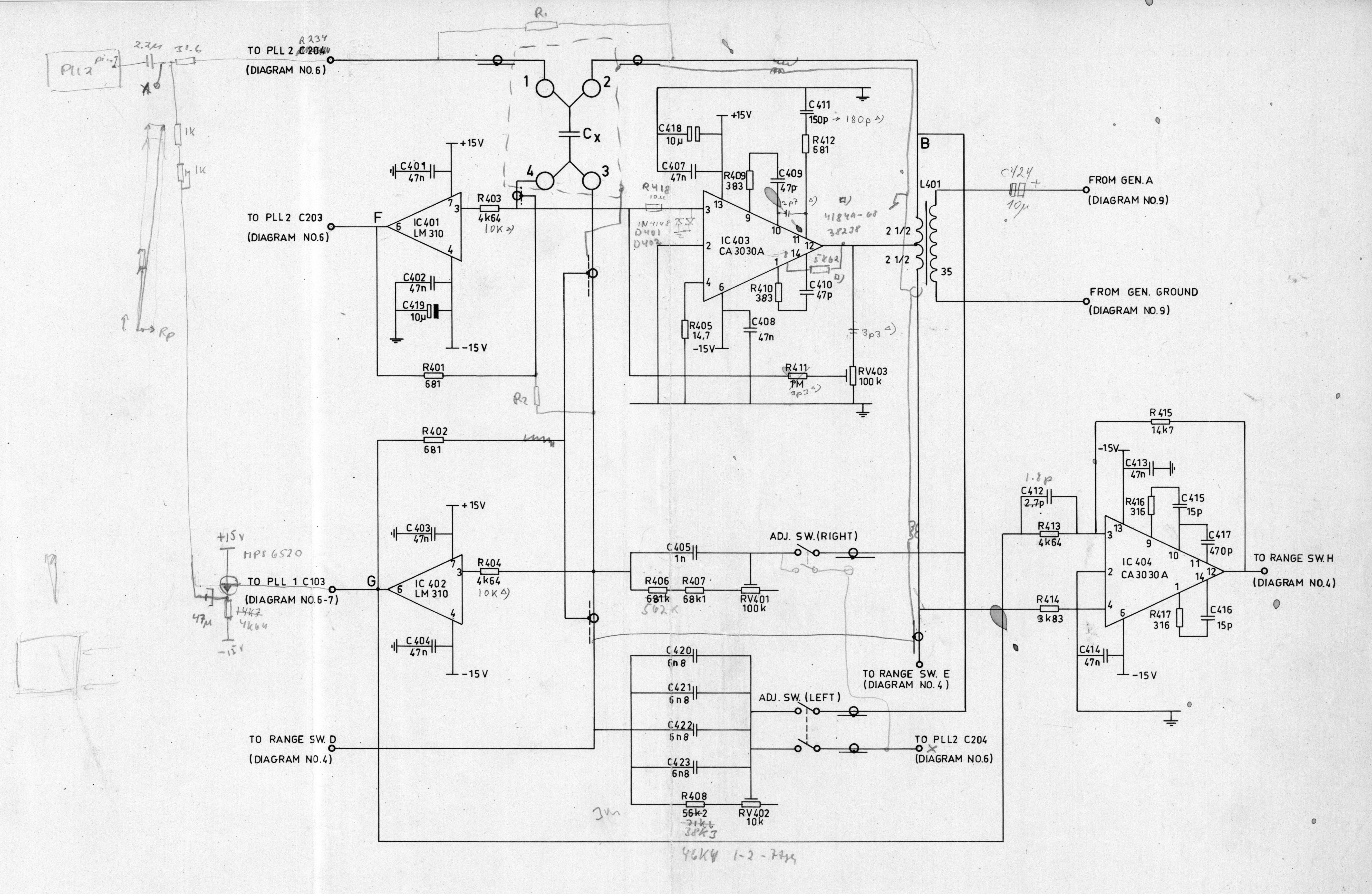
A/S DANBRIDGE.



72550-1	CLM 1 DIAGRAM NO. 1		
	SIMPLIFIED	RETTET	GODK.
A/S DANBRIDGE	BLOCK DIAGRAM	TEGNET :	110376 B. Ras.
		KONSTRUERET :	S. KOFOED OLSEN
		GODKENDT :	



72550-2	CLM 1 DIAGRAM NO.2		
	BLOCK DIAGRAM		
A/S DANBRIDGE		RETTET / GODK.	
		TEGNET :	120376 B. Ras.
		KONSTRUERET :	S. KOFOED OLSEN.
		GODKENDT :	

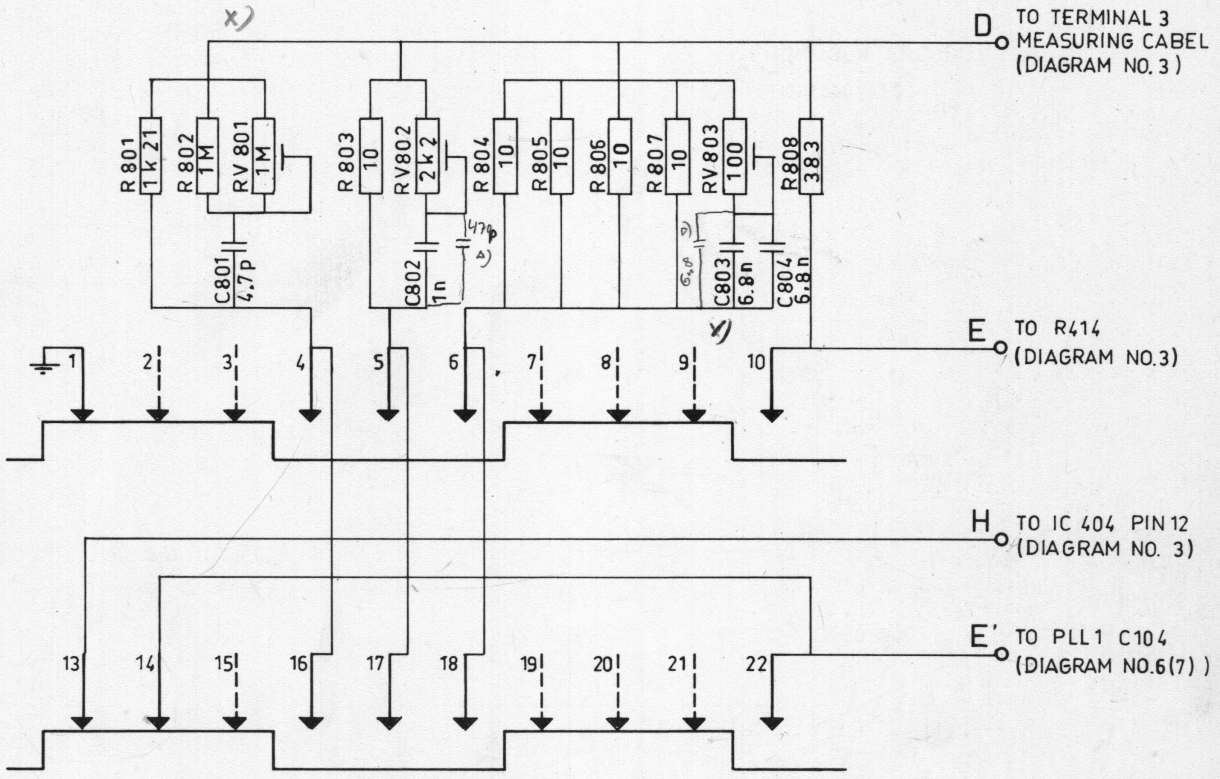


Δ) disse modificeringer indføres når ført ... monteres 21-9-77

R_1 og R_2 100 - 178 Ω typ 147 Ω
for at kompensere for induktiv kobling i måle kabler
sættes således ...
= 7×10⁻⁴ ± 10⁻⁴ 1-2-77

72550-3	CLM 1 DIAGRAM NO. 3	RETTET		5-10-76	
	MEASURING CIRCUIT	RETTET	GODK.		
		TEGNET:		180376 B. Ras.	
A/S DANBRIDGE		KONSTRUERET:		S. KOFOED OLSEN	
		GODKENDT:			

CAP RANGE F



RANGE

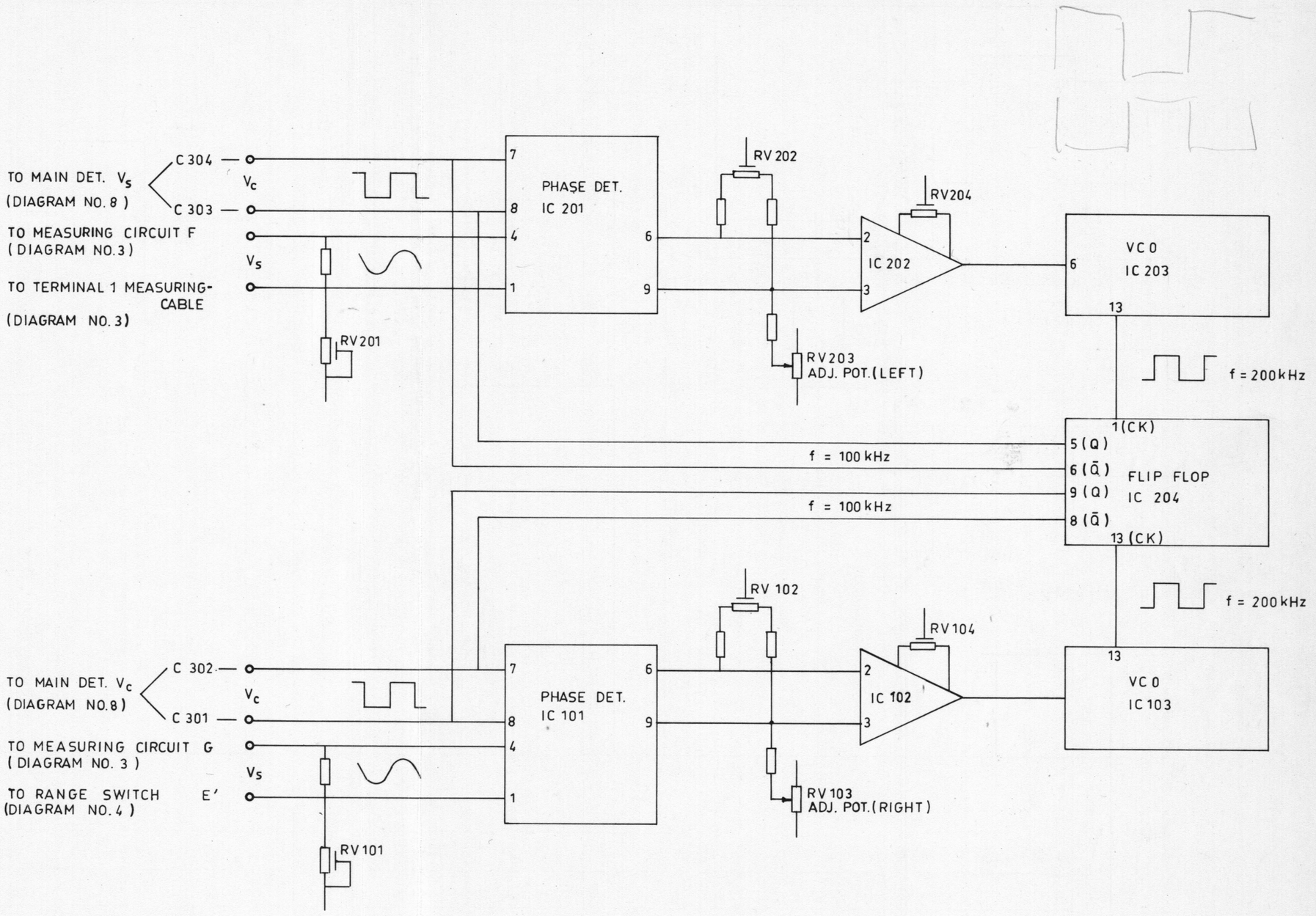
100p – 1n	R_{N_1}	=	R808	= 383 Ω
1n – 30n	R_{N_2}	=	R808 // R801	= 291 Ω
30n – 1µ	R_{N_3}	=	R_{N_2} // R803	= 9.66Ω
1µ – 25µ	R_{N_4}	=	R_{N_3} // R804 // R805 // R806 // R807	= 2.00Ω

x) R802 udgår
RV801 erstattet med 220kΩ pot 5-10-76 Hy.

a) Disse modificeringer indføres når ferritrørene indføres 21-9-77 Hy

x) Ændret fra 3x6n8 → 22n

72550-4	CLM1 DIAGRAM NO. 4		
	RANGE SWITCH	RETTET / GODK.	
A/S DANBRIDGE.		TEGNET :	190376 B.Ras.
		KONSTRUERET :	S.KOFOED OLSEN.
		GODKENDT :	



RV 103 and RV 203 is front panel multiturn potentiometers.

72550-5	CLM 1 DIAGRAM NO. 5		
	PLL SYSTEM		
A/S DANBRIDGE	BLOCK DIAGRAM	RETTET / GODK	
		TEGNET :	300376 B. Ras.
		KONSTRUERET :	S. KOFOED OLSEN
		GODKENDT :	

+15 V

C227 10µ

RV202 10k

R214 9k09 • R216 147k • R217 147k • R218 9k09 •

C214 22n · R226 2k15 · R227 1M

C215 47n

RV204 100 k

C222 10 µ

C223 220p

IC 203 XR2207CP

R232 5k62

R233 4k64

C225 1.5 µ

C220 33p

R229 5k62 · R230 6k81

IC 202 LM 725 C

R222 10 · R223 10

C210 2.2 µ · C211 2.2 µ

R219 12k1

C218 4.7 n

D201 1N4148 · D202 1N4148

C201 2.2 µ · C202 2.2 µ · C203 2.2 µ · C204 2.2 µ

C205 3.3p · C206 3.3p

R203 1k47 · R204 1k47

R208 178 · R211 178

IC 201 MC1596

R213 3k16

C207 10p · C208 10p

R210 46.4 · R212 46.4

R201 8k25 · R202 8k25 · R205 4k64

RV201 1k · R206 1k

R207 681 · R209 5k62

C209 0.47µ

R215 12k1

+5V

C224 47n · C226 47n

C219 10 µ · C221 47n

R231 1k

R220 1k · R224 1M · C213 22n · C216 47n · R228 100

RV203 1k

R221 3k16 · C212 0.1 µ · R225 2k15

14-12-11-10-4-3 and 2
1(CK)
13 (CK)
IC 204
SN 74 S 113 N
(Q) (Q̄) (Q̄) (Q)
7 5 6 8 9

C228 10µ

C217 10µ

-15V

Vc

Vs

TO PLL1 IC 103 PIN 13

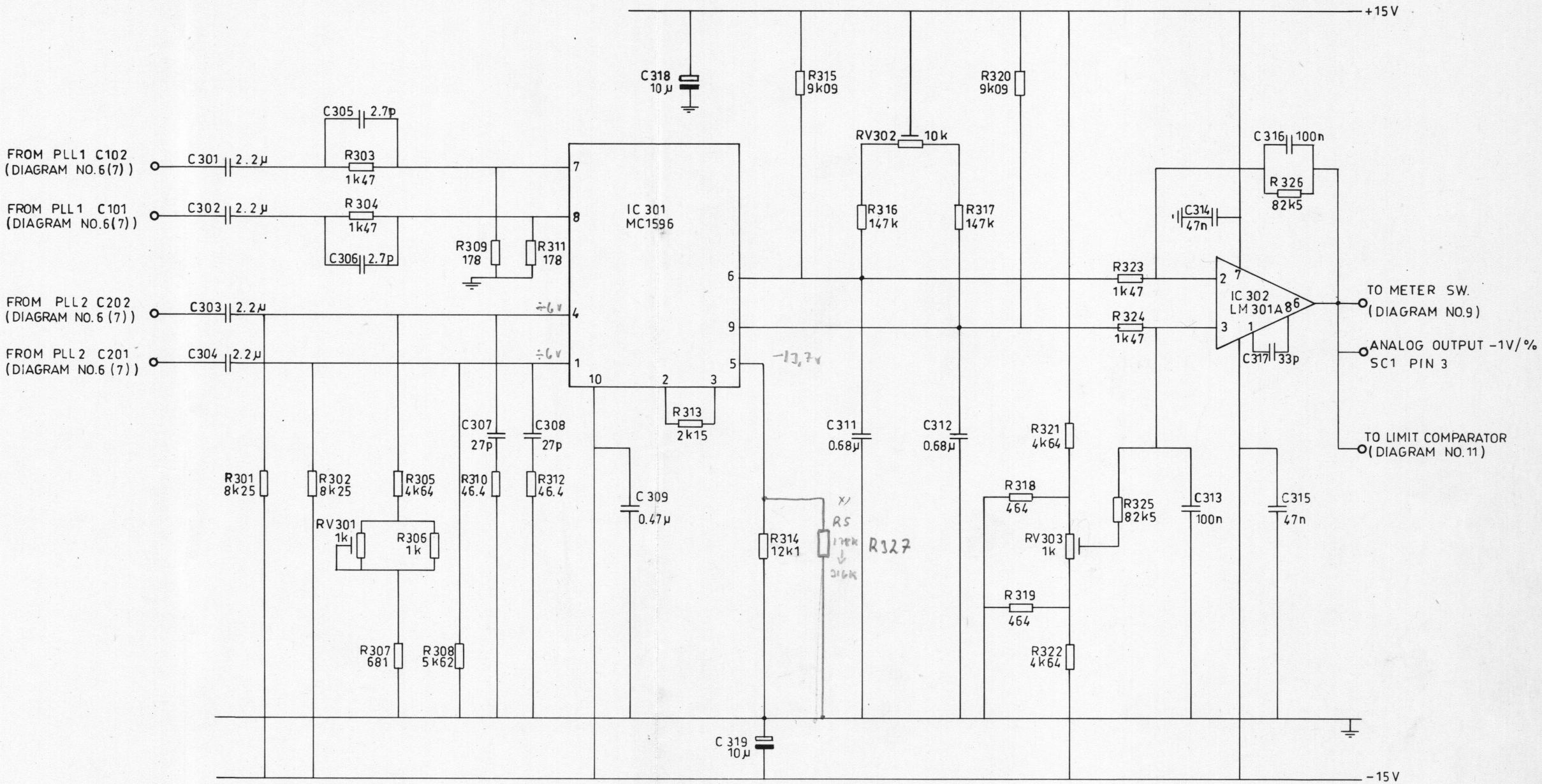
TO MAIN DET. C303 C304

TO PLL 1 C101 C102

• MATCHED RESISTORS
ΔR ≤ 0.1 %
ΔTC ≤ 5pp M/°C

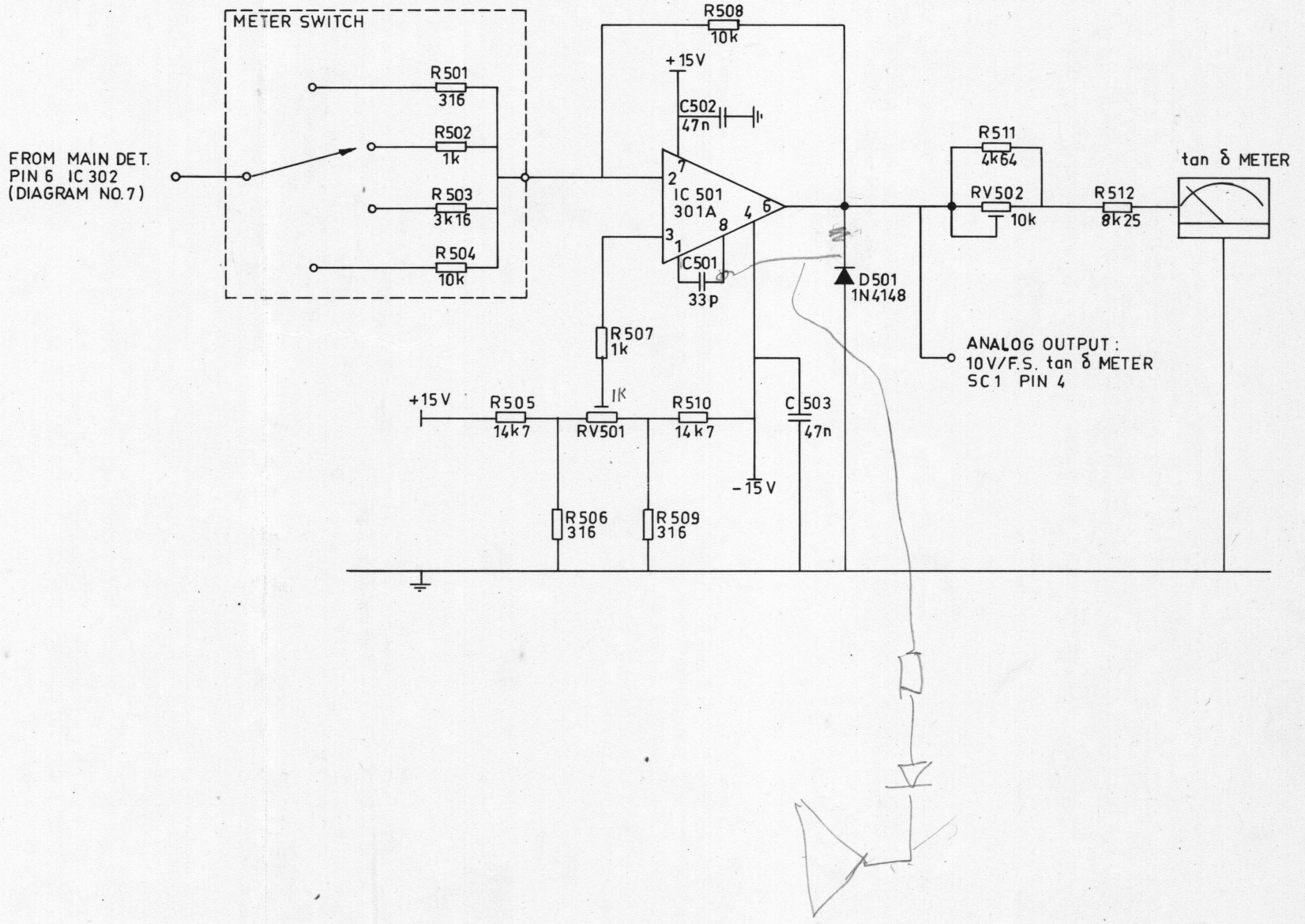
FOR PLL 1 REPLACE x 2xx WITH x1xx EXEPT FOR IC204 - C224 AND C226 WHICH ARE IN COMMON.

7255-6 (7)	CLM 1 DIAGRAM NO.6 (7)			
		RETTET	GODK.	
A/S DANBRIDGE.	PHASE LOCK 100p 2. (&1)	TEGNET:		150676 B.Ras.
		KONSTRUERET :		S.KOFOED OLSEN.
		GODK.:		

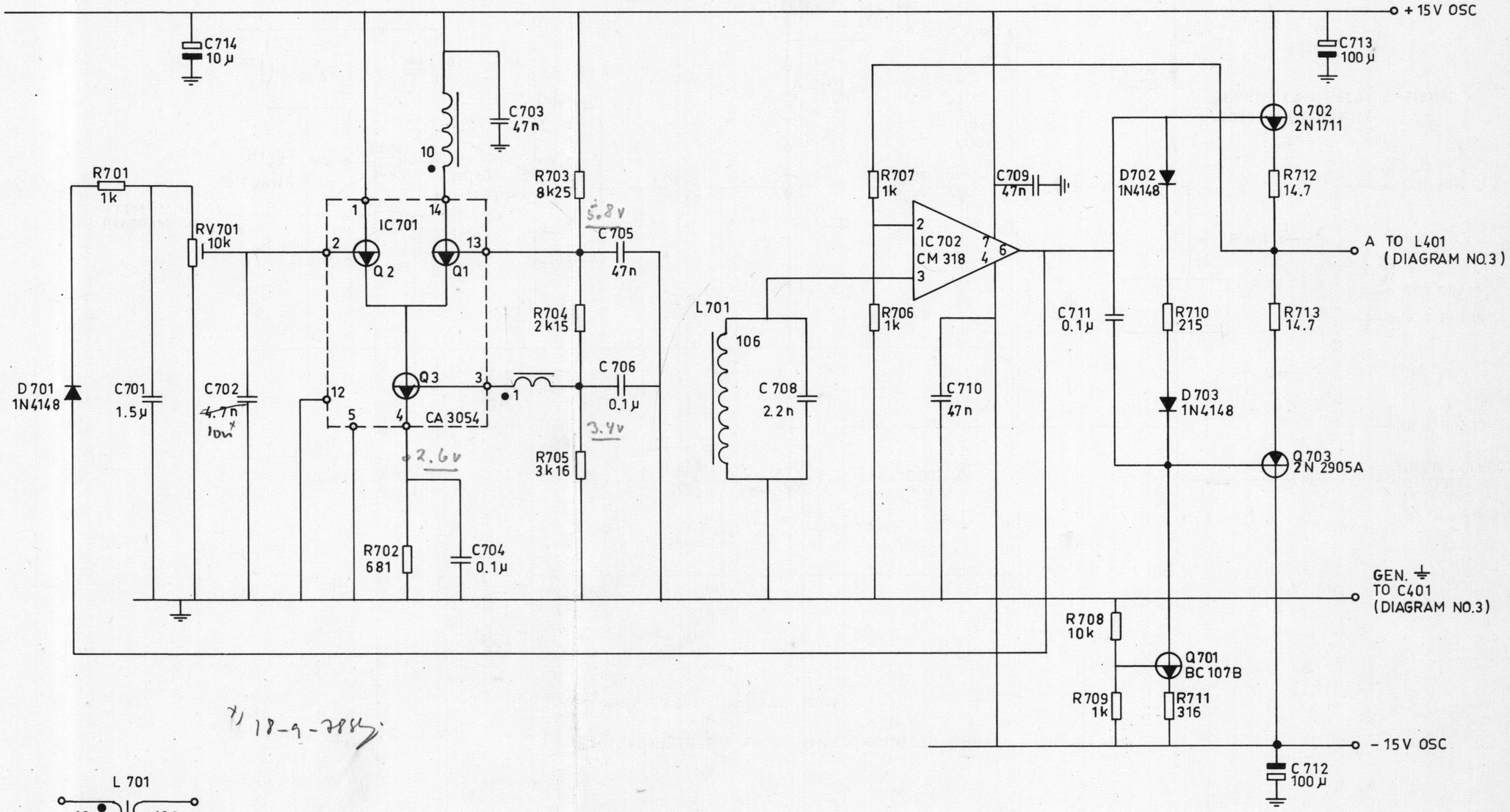


X) Rs sætter følsomheden af Main Det
således at vi får de korrekte V/rad. 2-2-72Sh.

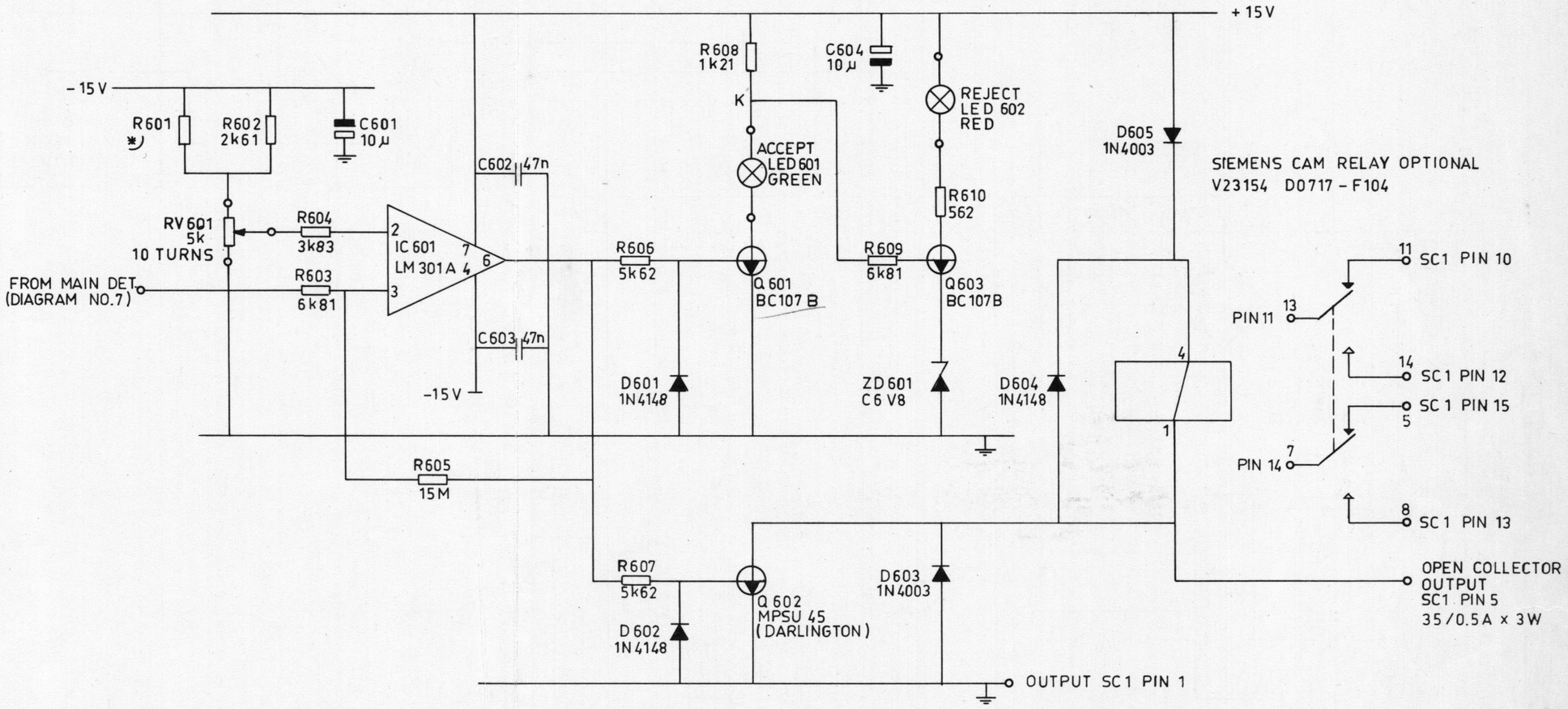
72550-8	CLM1 DIAGRAM NO.8			
		RETTET	GODK.	
A/S DANBRIDGE	MAIN DETECTOR	TEGNET	010476 B.Ras.	
		KONSTRUERET:	S.KOFOED OLSEN	
		GODK.		



72550-9	CLM 1 DIAGRAM NO.9		
		RETTET	GODK.
A/S DANBRIDGE	METER AMPLIFIER	TEGNET	160676 B.Ras.
		KONSTRUERET :	S. KOFOED OLSEN
		GODK.:	



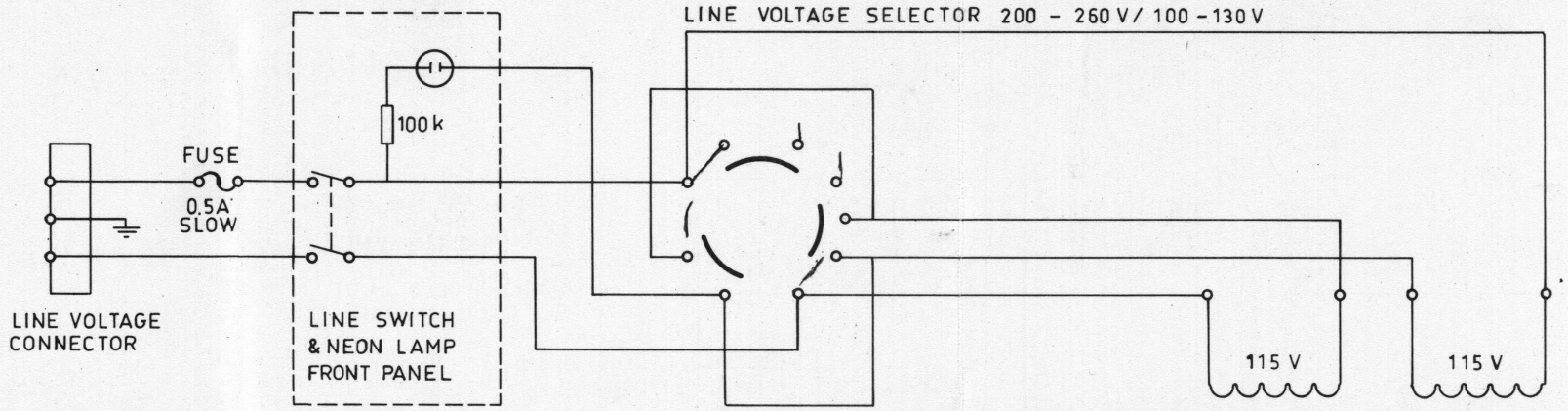
72550 - 10	CLM 1 DIAGRAM NO. 10		
A/S DANBRIDGE	GENERATOR	RETTET / GODK.	
		TEGNET	170676 B.Ras.
		KONSTRUERET :	S. KOFOED OLSEN.
		GODK.:	

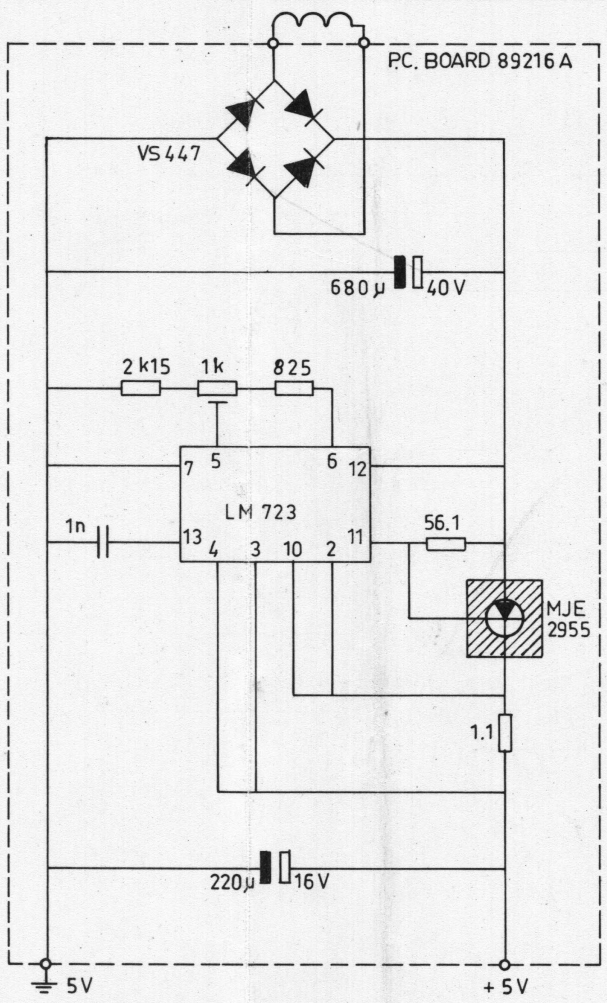


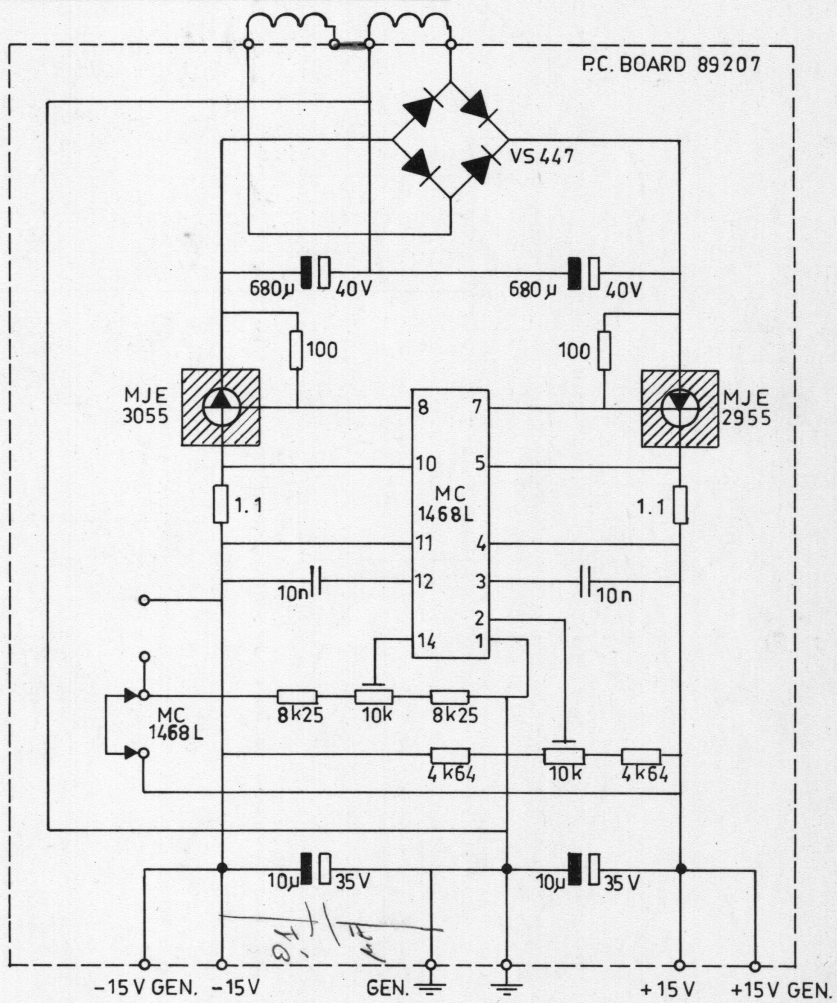
SC1 ARE PLACED ON REAR PANEL

*) R601 ADJUSTS THE FRONT PANEL MOUNTED DIGITAL KNOB READING

72550-11	CLM 1 DIAGRAM NO.11		
A/S DANBRIDGE	LIMIT COMPARATOR	RETTET GODK.	
		TEGNET :	210676 B.Ras.
		KONSTRUERET :	S. KOFOED OLSEN
		GODK. :	







72550-12	CLM 1 DIAGRAM NO.12		
		RETTET	GODK.
A/S DANBRIDGE.	POWER SUPPLY	TEGNET :	220676 B.Ras.
		KONSTRUERET !	S.KOFOED OLSEN
		GODK.	